**ASSIGNMENT-1**

**SUBJECT: DIGITAL LOGIC DESIGNING (LAB)**

**TOPIC: Proteus Designs**



**Submitted to: Sir Irfan**

**Submitted by: Muhammad Shahzad Akbar**

**Major: BSCS**

**Roll No: 0233-BSCS-22**

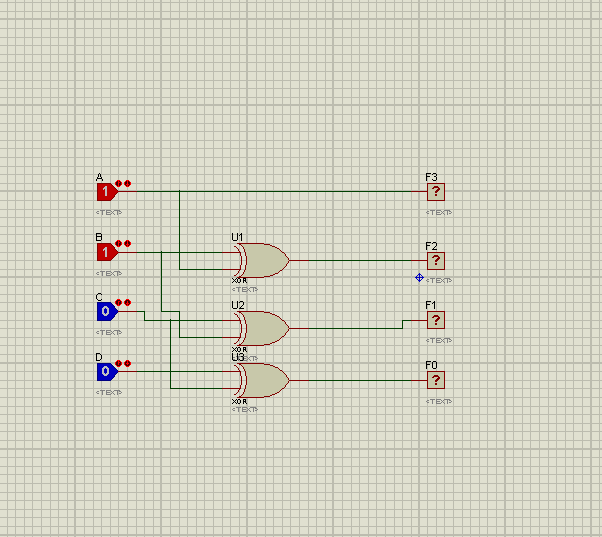
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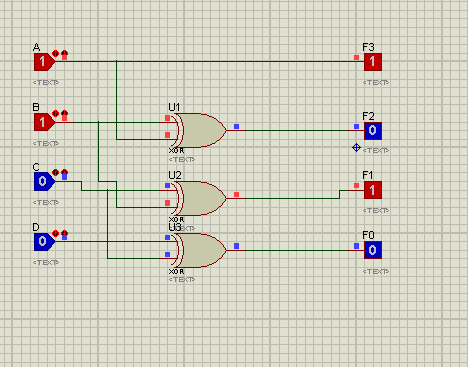
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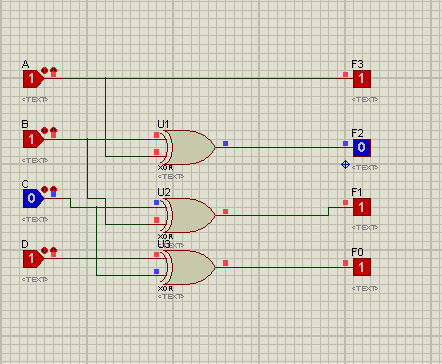
**Task 1:**

**--> Binary to Gray Code Converter.**

This circuit converts a binary input to its corresponding Gray code representation, where only one bit changes between consecutive values

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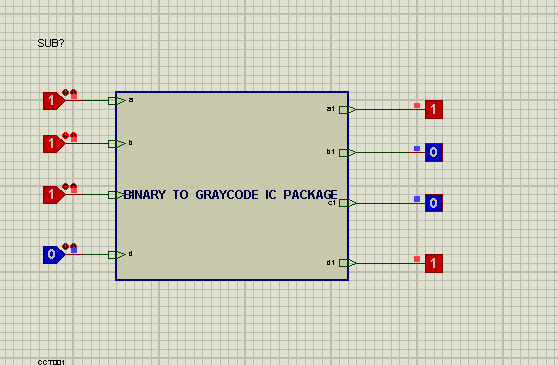
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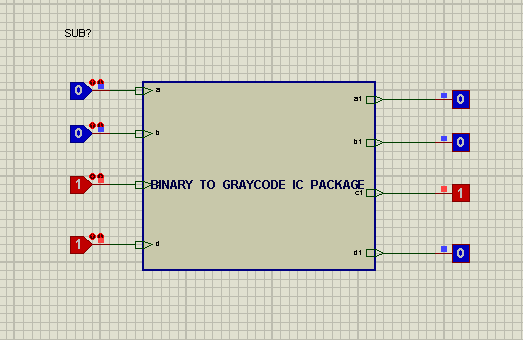
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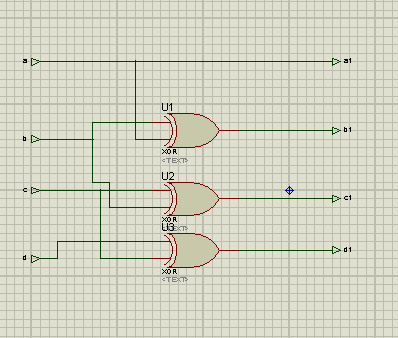
**Task 2:**

**--> Design IC Package Binary to Gray Code Converter.**

This is the IC package of Binary to GrayCode circuit that converts a binary input to its corresponding Gray code representation, where only one bit changes between consecutive values

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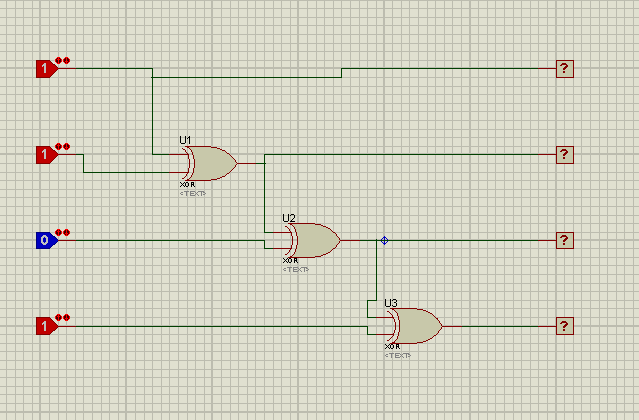
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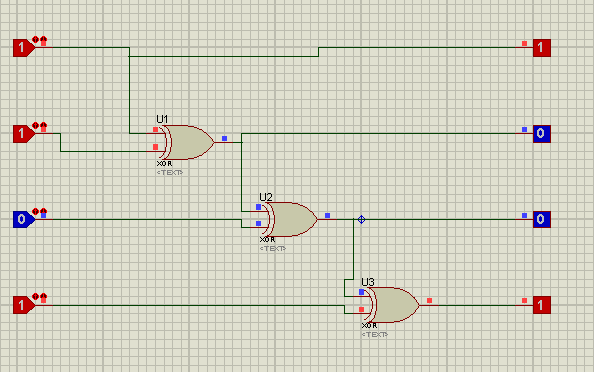
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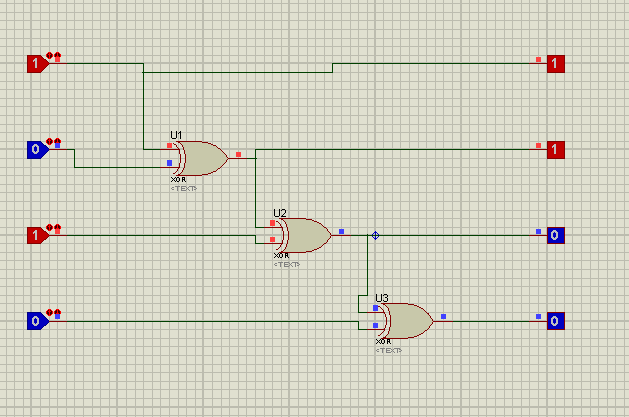
**Task 3:**

**--> Gray to Binary Code Converter.**

This circuit converts a Gray code input to its equivalent binary representation, determining the corresponding value by considering the changing bits in sequence.

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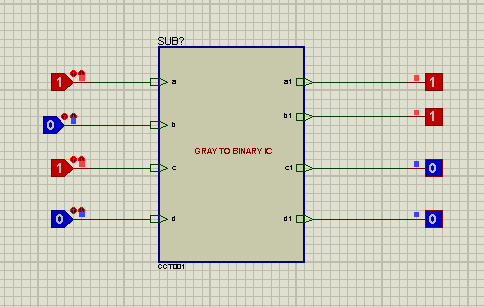
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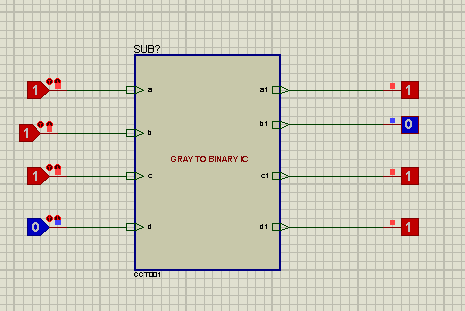
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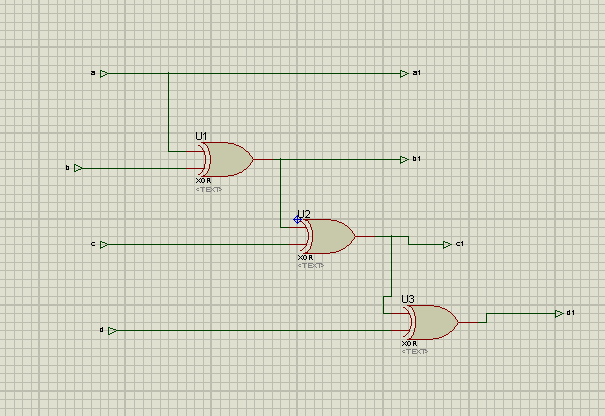
**Task 4:**

**--> Design IC Package Gray to Binary Code Converter.**

This is the IC package of the Gray to Binary Code circuit that converts a Gray code input to its equivalent binary representation, determining the corresponding value by considering the changing bits in sequence.

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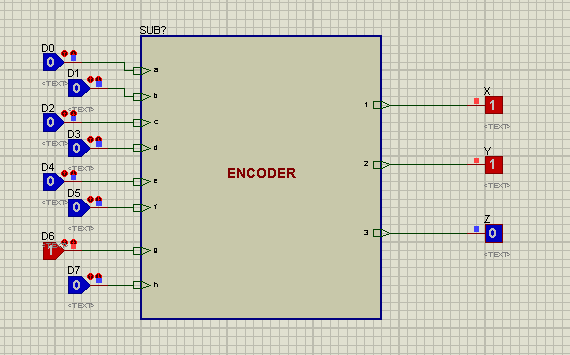
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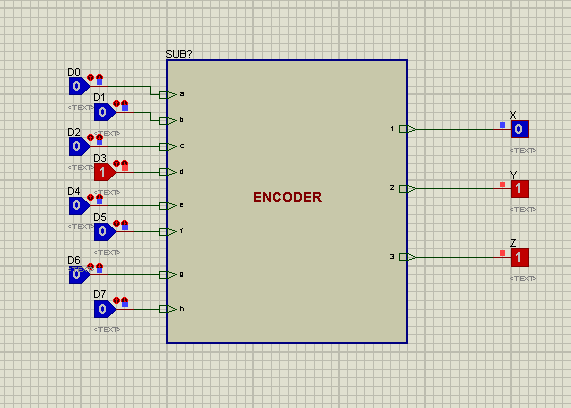
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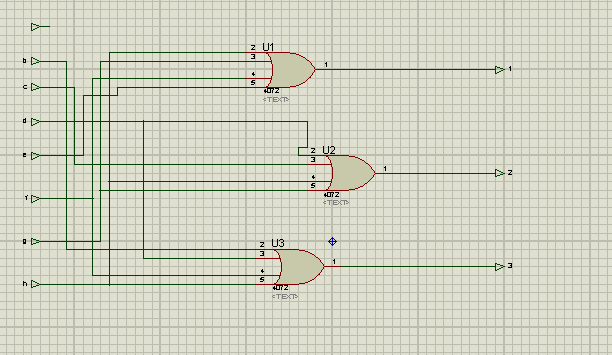
**Task 5:**

**--> Design IC Package of Encoder.**

The IC package for an encoder is a compact integrated circuit that encodes a set of input signals into a binary code. This package is designed to efficiently process and convert multiple input lines into a corresponding binary output, which is useful in various digital applications.

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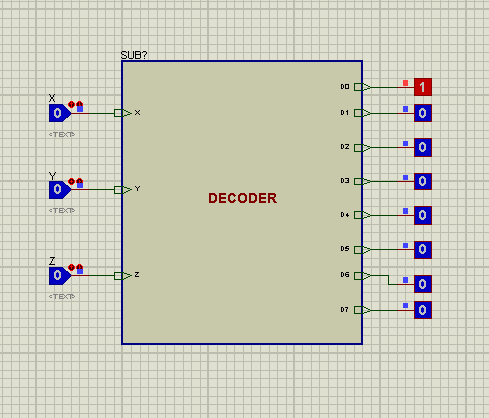
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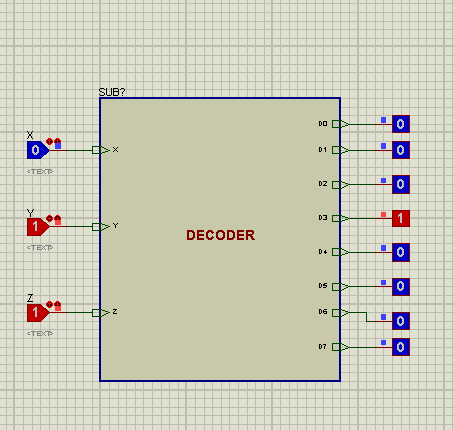
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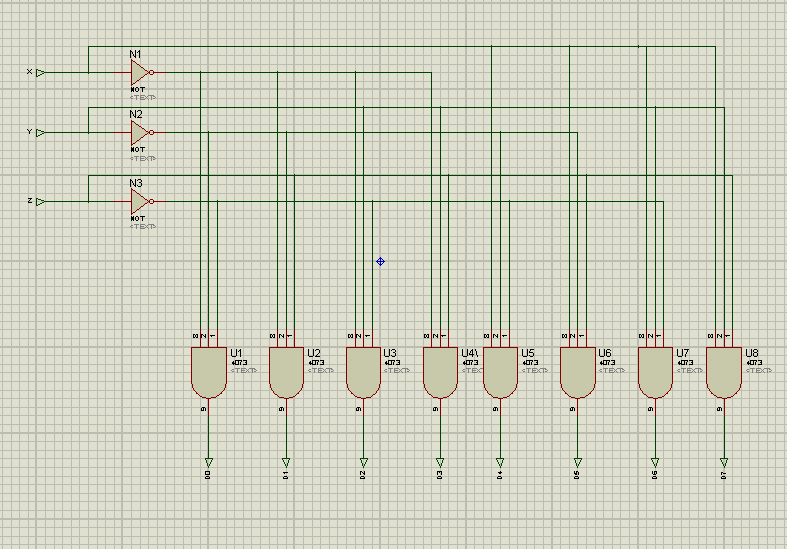
**Task 6:**

**--> Design IC Package of Decoder.**

The IC package of a decoder is a specialized integrated circuit designed to take binary input codes and activate a specific output line based on the binary input value. This package is essential for converting binary codes into corresponding output signals in applications such as demultiplexing and control systems.

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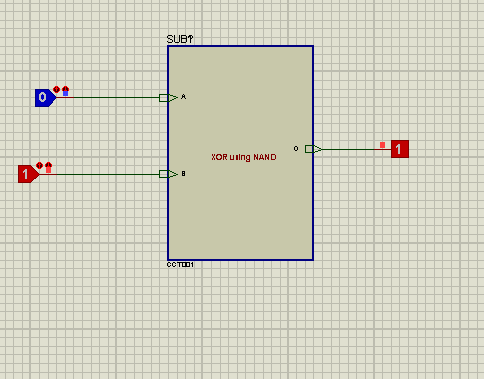
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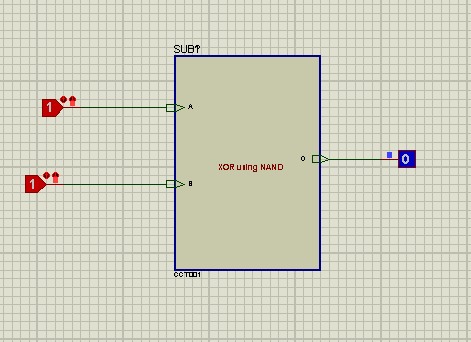
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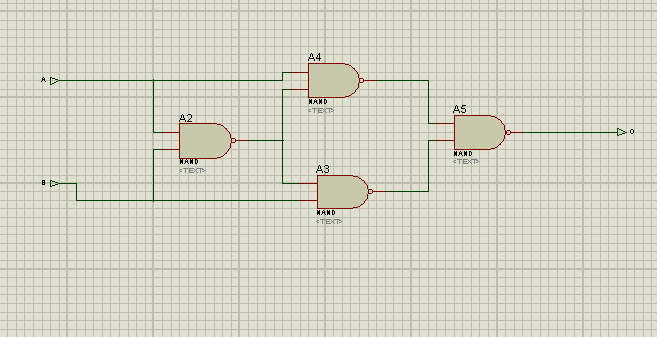
**Task 7:**

**--> Design IC Package of XOR using NAND Gates.**

The IC package of an XOR gate implemented using NAND gates combines multiple NAND gates to create a logic circuit that produces an XOR (exclusive OR) function. This package offers an efficient way to perform XOR operations by utilizing the properties of NAND gates.

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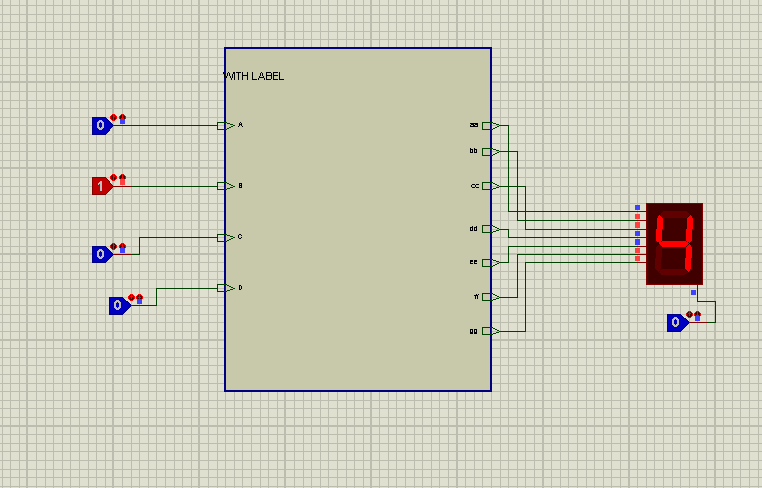
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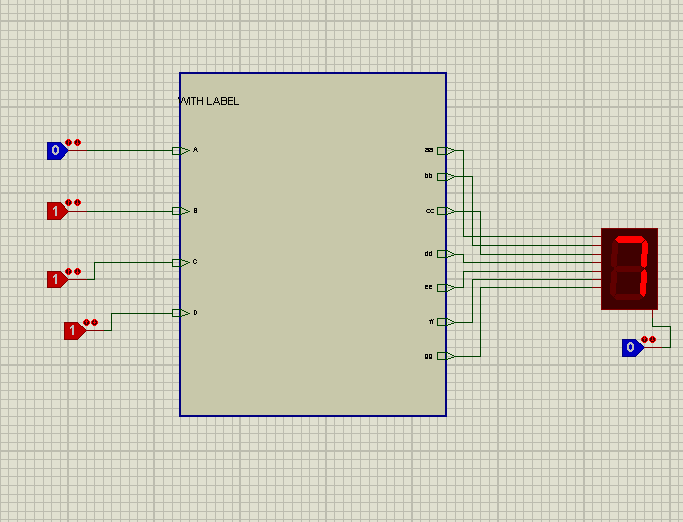
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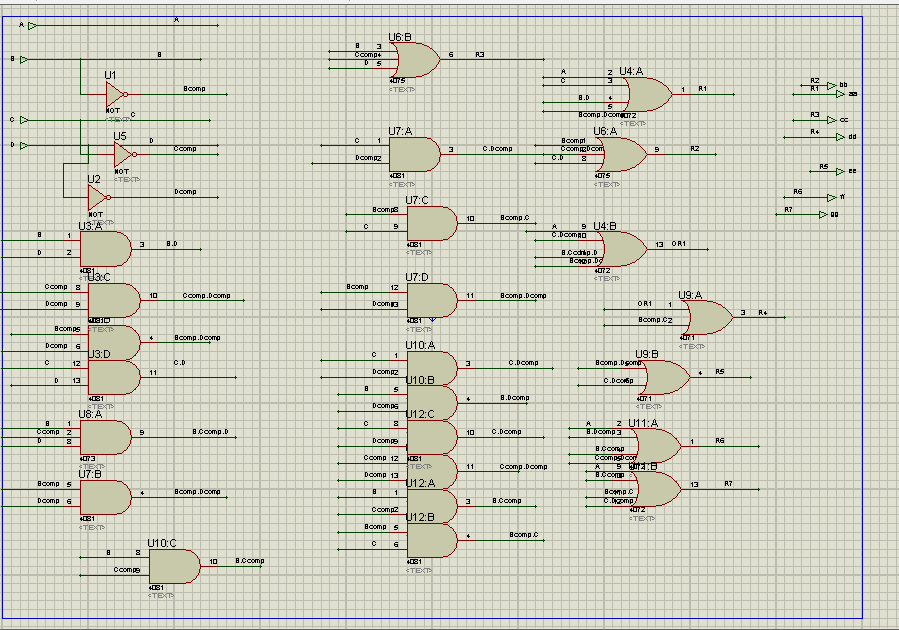
**Task 8:**

**--> Design BCD to 7 Segment.**

The BCD to 7 Segment Decoder circuit converts Binary-Coded Decimal (BCD) input values into corresponding signals that drive a 7-segment display. This enables the display of decimal digits from 0 to 9 on the 7-segment display, making it a fundamental component for visualizing numeric data.

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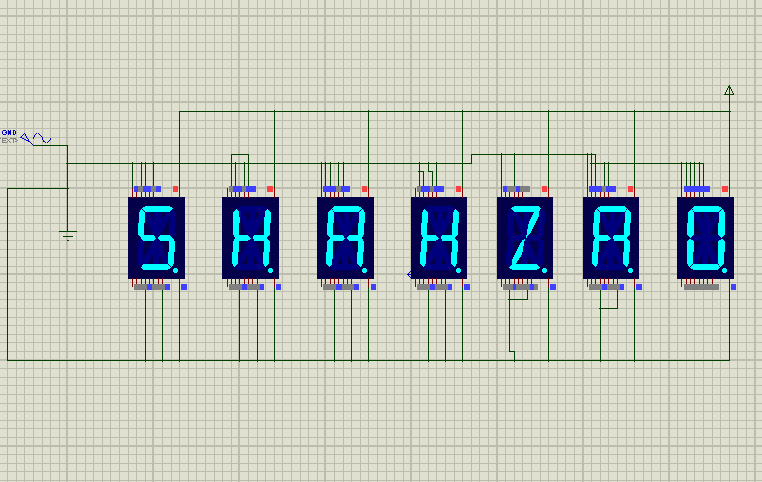
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**Task 9:**

**--> Display your Name using 14 Segment.**

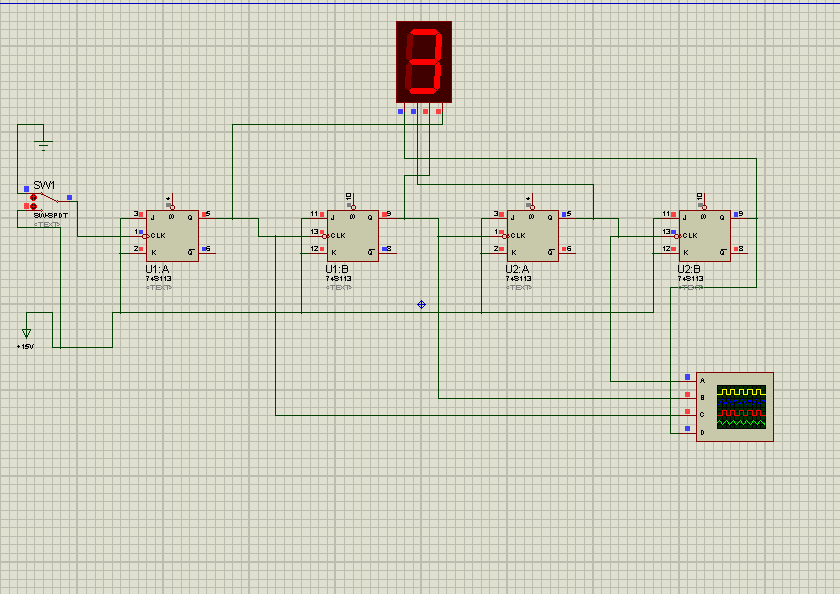
The 'Display Name using 14 Segment' circuit is designed to showcase alphanumeric characters, including letters from the alphabet, numerals, and symbols, on a 14-segment display. By controlling each segment individually, this circuit allows for the versatile presentation of text and characters, making it suitable for various applications requiring advanced visual representation

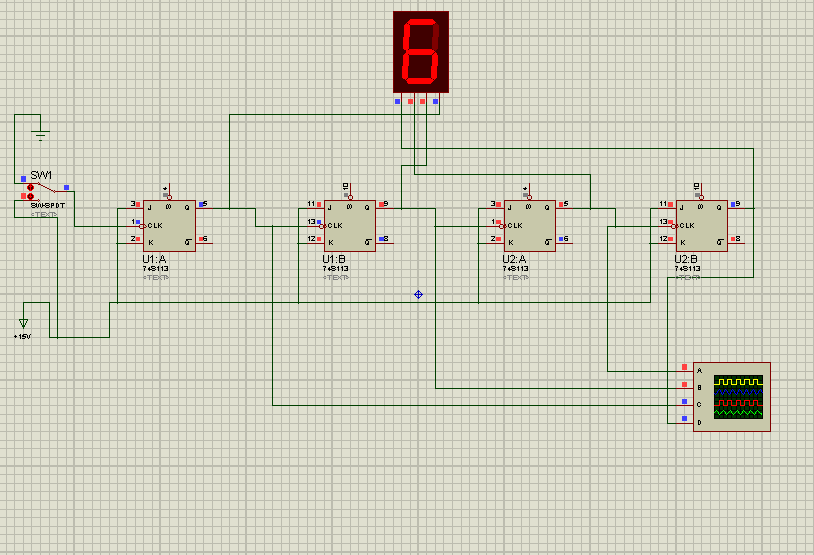
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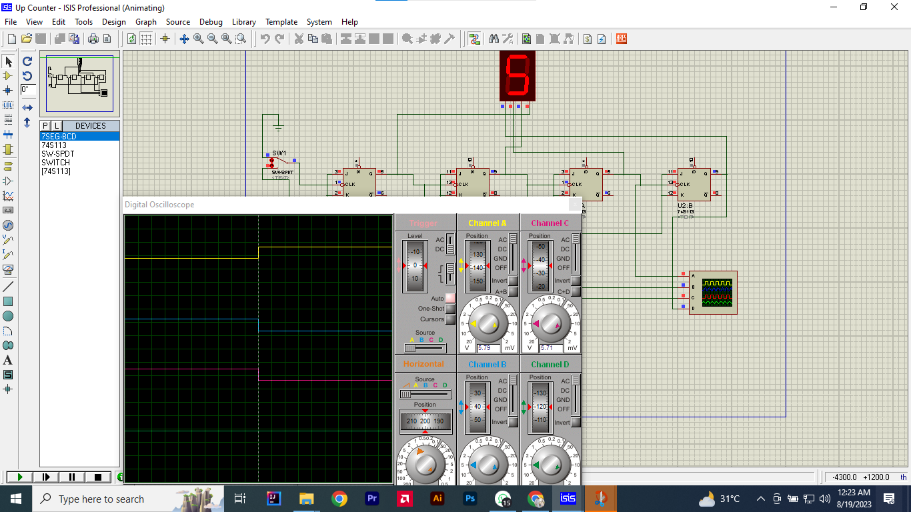
**Task 10:**

**--> Make an Up Counter.**

The Up Counter circuit is a sequential digital circuit that counts upwards in binary representation with each click. It increments its output value by one with every input, making it suitable for applications where counting and tracking events or occurrences are essential.

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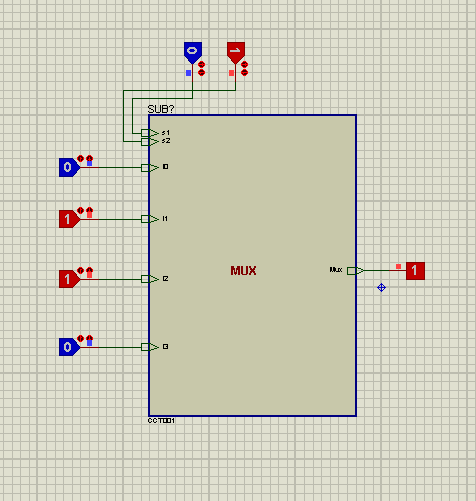
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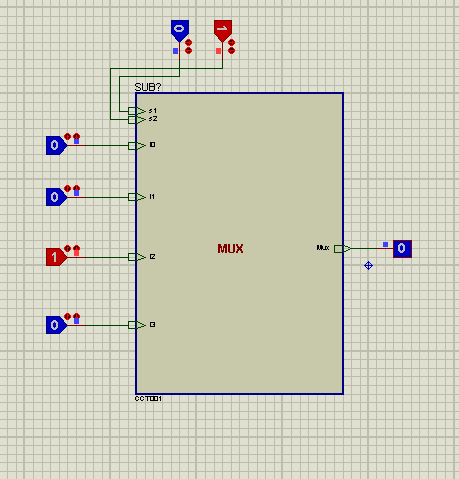
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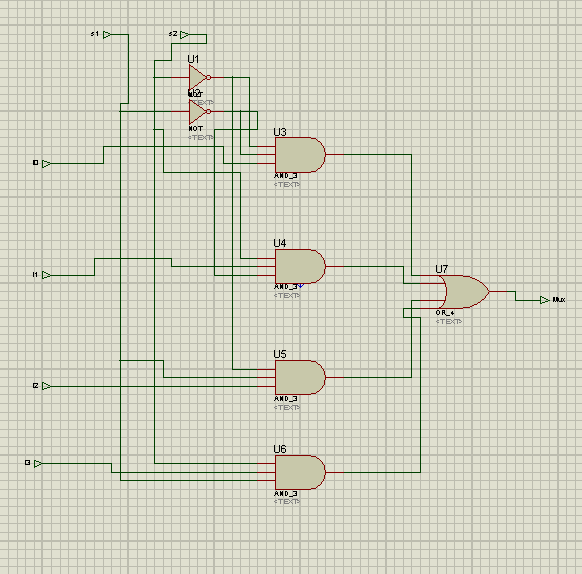
**Task 11:**

**--> Design IC package of Multiplexer (4x1).**

The IC package of a 4x1 Multiplexer integrates four input lines and one output line, along with select inputs. This package efficiently selects and forwards one of the four input signals to the output based on the select inputs, allowing for versatile signal routing and data selection in digital circuits.

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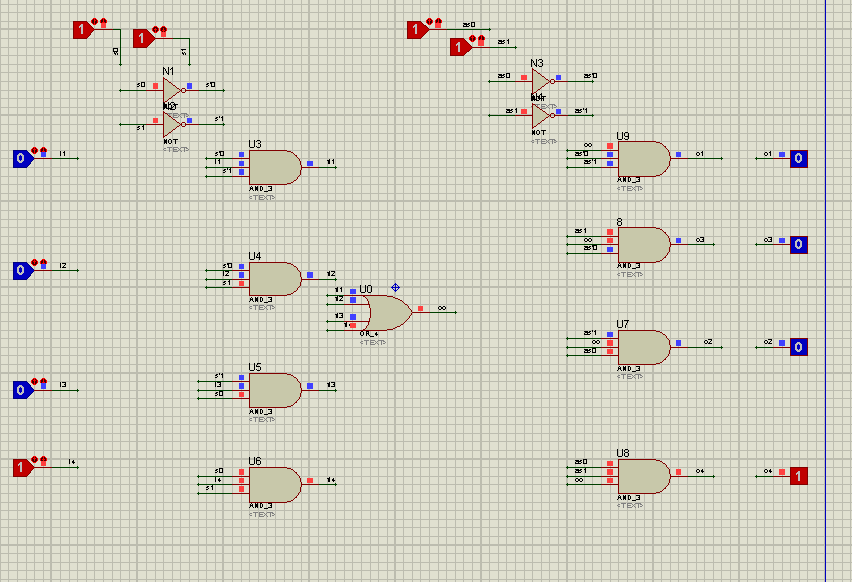
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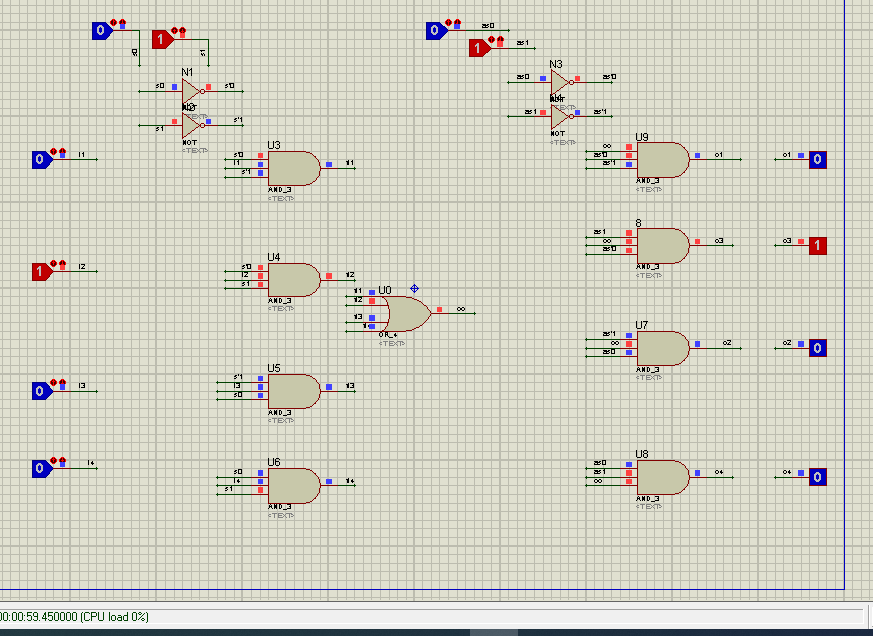
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**Task 12:**

**--> Design Multiplexer (4x1) to Demultiplexer by Labeling.**

The process of converting a 4x1 Multiplexer to a Demultiplexer through labeling involves redefining the select inputs and output of the multiplexer. By assigning meaningful labels to inputs and using the multiplexer's select inputs to control the routing, the circuit now functions as a demultiplexer, distributing a single input signal to one of the four output lines based on the select inputs.

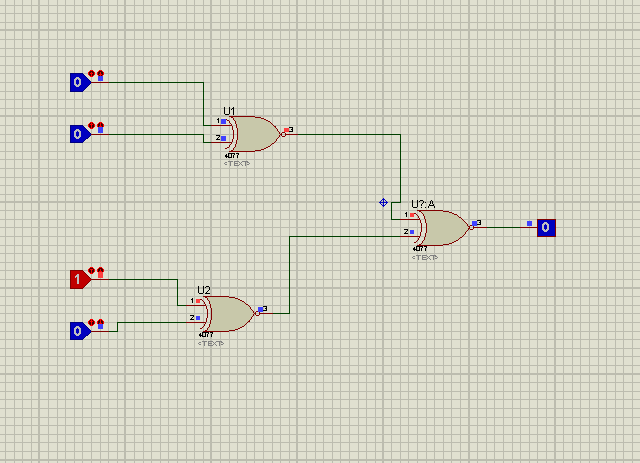
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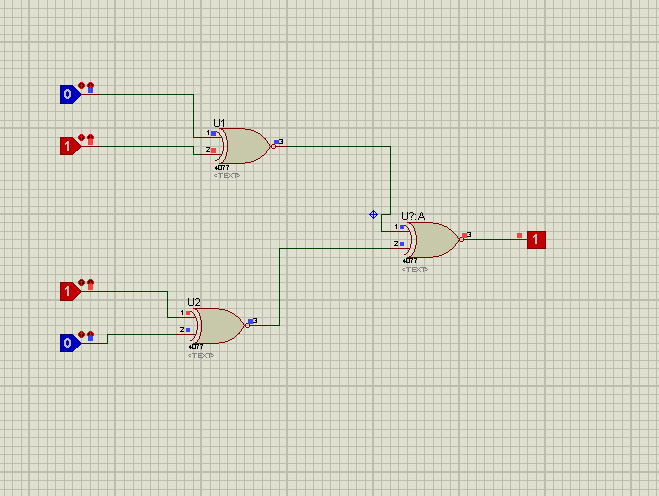
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**Task 13:**

**Odd parity checker**

The Odd Parity Checker circuit examines a set of binary input bits and determines whether the count of '1' bits is odd or even. If the count is even, the circuit outputs a logic '0'; if odd, it outputs a logic '1'. This circuit is used to verify data integrity by ensuring an odd number of '1' bits in a binary sequence.

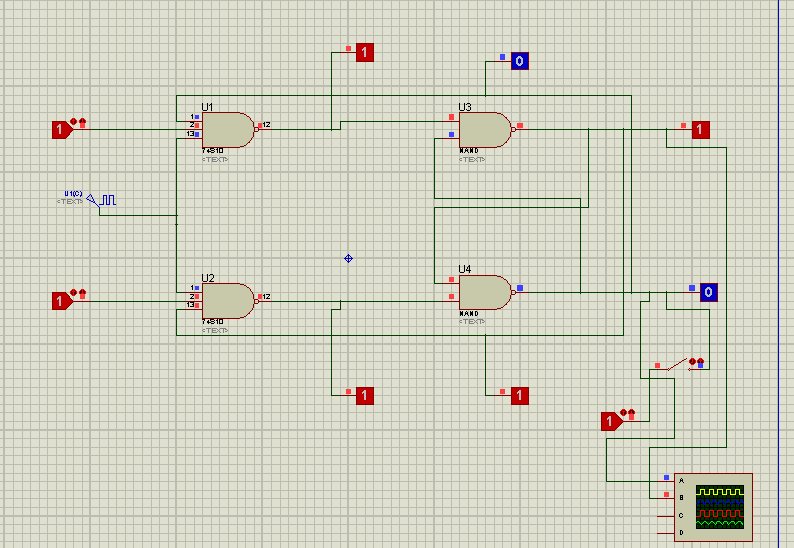
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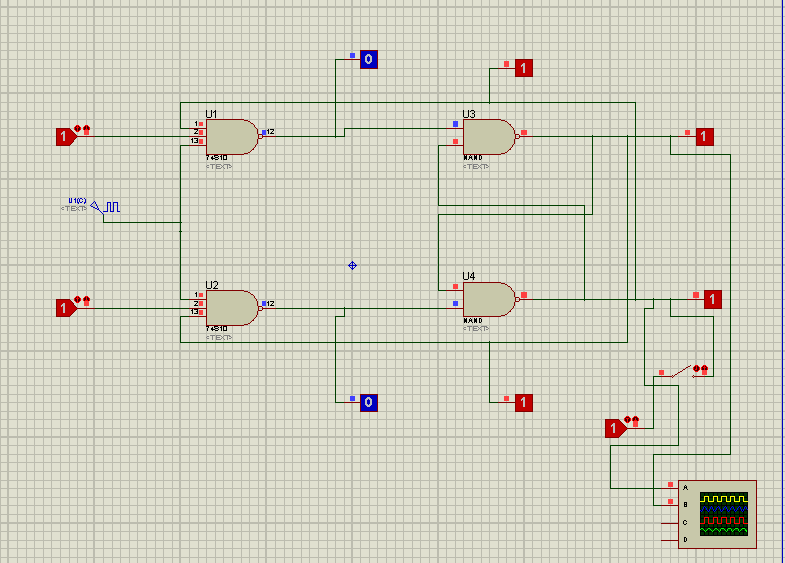
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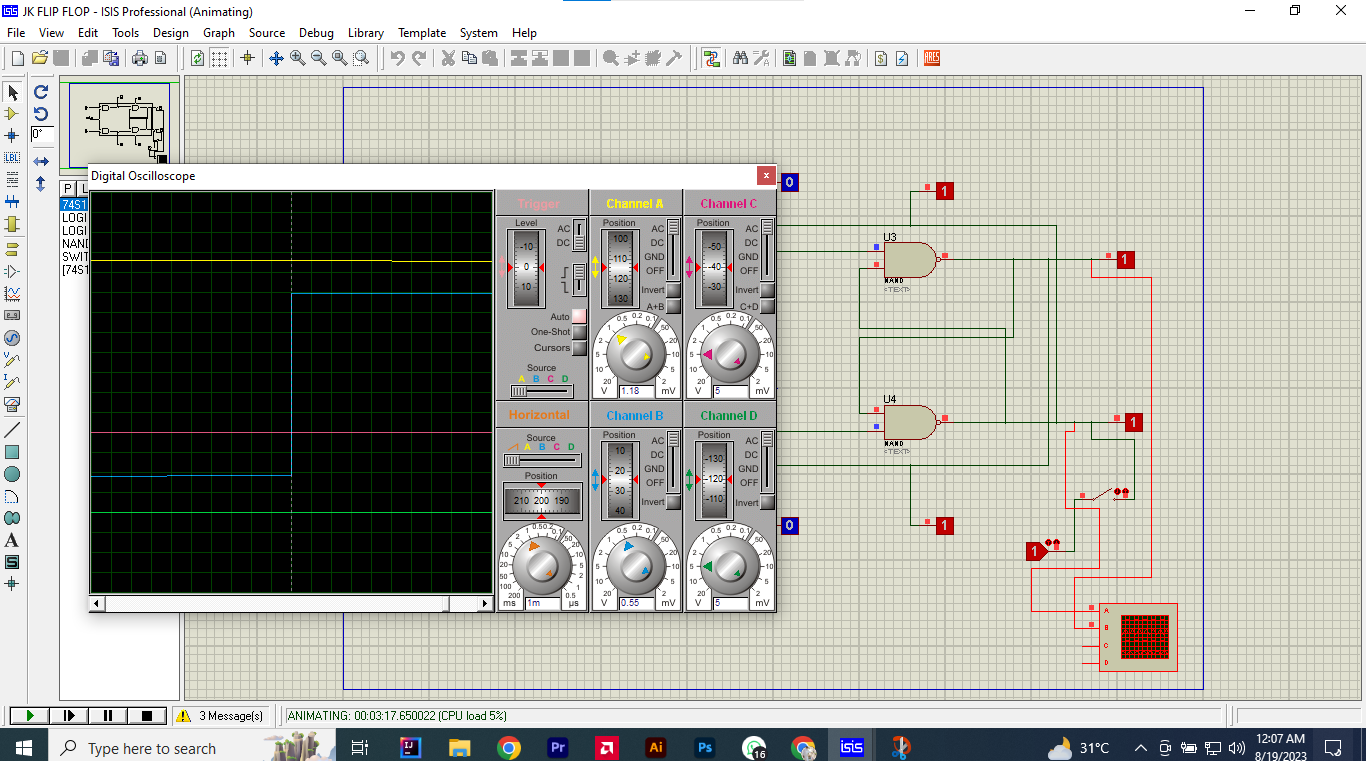
**Task 14:**

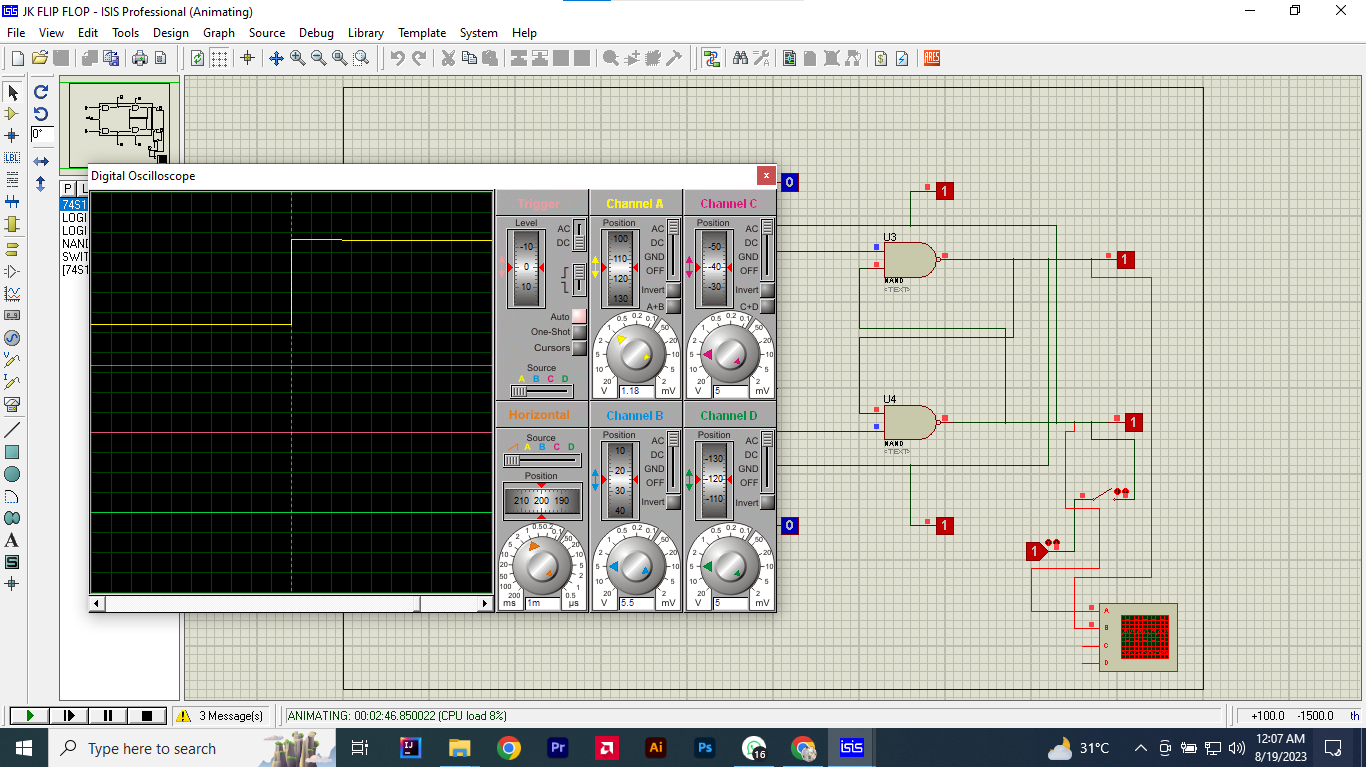
**JK flip flop**

The JK Flip-Flop is a sequential logic circuit with two inputs, J (set) and K (reset), and two outputs, Q and Q̅. It is capable of toggling its output states based on clock pulses and the values of its inputs. The JK Flip-Flop is widely used for memory storage, frequency division, and sequential circuit applications.

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